REMARKS

In the Official Action mailed 06 January 2006, the Examiner reviewed claims 1-17. The Examiner has provisionally rejected claims 1, 3-6 and 10-17 for double patenting; has objected to claim 17 under 37 C.F.R. §1.75(c); has rejected claims 1 and 2 under 35 U.S.C. §102(e); has rejected claim 7 under 35 U.S.C. §103(a); and has rejected claims 8 and 9 under 35 U.S.C. §103(a).

Applicant has amended claim 1. Claims 1-17 remain pending.

The rejections are respectfully traversed below, and reconsideration is requested.

Provisional Rejection of Claims 1, 3-6 and 10-17 for Double Patenting

The Examiner has provisionally rejected claims 1, 3-6 and 10-17 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 2-5, 9, 10 and 12-17 of copending Application No. 10/699,764, which was filed on the same day as the present application, and includes the same inventors.

Applicant submits herewith a terminal disclaimer to obviate the provisional double patenting rejection over the referenced co-pending application, and requisite fee. Applicant also submits a terminal disclaimer for the related application US 10/699,766 which is commonly owned with the instant application.

Accordingly, reconsideration of the rejection of claims 1, 3-6 and 10-17 is respectfully requested.

Rejection of Claim 17 Under 37 C.F.R. §1.75(c)

The Examiner has rejected claim 17 under 37 C.F.R. §1.75(c) as being of improper independent form for failing to further limit the subject matter of claim 1 from which it depends. Applicant respectfully requests reconsideration in view of the amendment to claim 1.

Claim 1 recites a "processor ... which fetches and executes instructions." Such a processor, as described in the specification may comprise dedicated logic circuitry as shown in Fig. 1 and described in paragraph [0030], or may comprise as stated in claim 17, "a configurable logic array configured to execute said instructions" (Fig. 2, paragraph [0032]). Thus, claim 17 recites a species of the more generic claim 1, and therefore "further limits" claim 1.

Accordingly, reconsideration of the objection to claim 17 is respectfully requested.

Rejection of Claims 1 and 2 under 35 U.S.C. §102(e)

The Examiner has rejected claims 1 and 2 under 35 U.S.C. §102(e) as being anticipated by Allegrucci (U.S.. Pat. No. 6,792,527). Applicant respectfully requests reconsideration in view of the amendment to claim 1.

In particular, Claim 1 requires that the memory store two types of program, including "... instructions for a mission function for the integrated circuit, instructions for a configuration load function used to receive configuration data via said input port, and ... instructions for an initialization function used to transfer the configuration data to the programmable configuration points within the configurable logic array in response to an initialization event..."

Allegrucci on the other hand does not describe the initialization function process, except to show a "Configuration Unit" in Figure 1. There is no text describing the operation of the Configuration Unit in Allegrucci. The fact that the "Configuration Unit" in Allegrucci is illustrated as a block separate from the microprocessor 105 and associated memory 110 in fact suggests that the processor in the Allegrucci system does not execute the "initialization function" process. The Examiner cites column 3, lines 28-41 and column 1, line 66 to column 2, line 4 as corresponding to the three types of program recited in claim 1. However, the Examiner is mistaken. The cited passages appear to relate only to mission function programs. Column 3, lines 28-41 describe use of an initialization boot ROM and downloading initialization code and data from external memory. There is no mention of the "initialization function used to transfer the configuration data to the programmable configuration points within the configurable logic array in response to an initialization event" in this cited passage. Column 1, line 66 to column 2, line 4 describes the microprocessor 105 and its memory 110. There is no description of the "initialization function" processes in this cited passage. Accordingly, claim 1 is not anticipated by Allegrucci.

The Examiner also cites column 2, lines 55-64 as corresponding to the "processor" recited in claim 1. This passage describes various types of external memory in which instructions for the processor may be stored. It does not relate to the "initialization function" recited in claim 1.

Claim 2 depends from claim 1, and is patentable for at least the same reasons.

Accordingly, reconsideration of the rejection of claims 1 and 2 as amended is respectfully requested.

Rejection of Claim 7 under 35 U.S.C. §103(a)

The Examiner has rejected claim 7 under 35 U.S.C. §103(a) as being unpatentable over Allegrucci as applied to claim 1 above, and further in view of Robb et al. (Pat. No. 5,276,839). Claim 7 depends from claim 1, as amended, and therefore is patentable for the reasons discussed above and because of the unique combination recited.

Accordingly, reconsideration of the rejection of claim 7 is respectfully requested.

Rejection of Claims 8 and 9 under 35 U.S.C. §103(a)

The Examiner has rejected claims 8 and 9 under 35 U.S.C. §103(a) as being unpatentable over Allegrucci as applied to claims 1 and 20 above, and further in view of Sun et al. (Pat. No. 5,901,330). Claims 8 and 9 depend from claim 1, as amended, and therefore are patentable for the reasons discussed above and because of the unique combinations recited.

Accordingly, reconsideration of the rejection of claims 8 and 9 is respectfully requested.

Other References

The Examiner stated on page 4 of the Office Action, that "other" prior art in the Office Action could be used as a ground for rejection of claims 1 and 20. In particular, the Examiner mentioned the two Sun et al. patents, which are patents that also include Mr. Sun as a co-inventor. Applicant has reviewed the other references in the record and does not believe that they could be applied to render the present claims unpatentable. Accordingly, reconsideration of the statement is requested.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 1521-1).

Respectfully submitted,

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